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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): NVIDP235/P000846

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on June 20, 2006

Signature: Erica L. Farlow

Typed or printed name: Erica L. Farlow

Application Number	Filed
10/633,021	07/31/2003

First Named Inventor: Inderjit Singh et al.

Art Unit	Examiner
2811	Vu, Hung K.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [x] attorney or agent of record. Registration number 41,429
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

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NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of _____ forms are submitted.

REMARKS

Claims 1, 2, 4-18, 20, 21, 27, 29 and 30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Specifically, the Examiner argues that the specification does not disclose an entirety of at least one of the transistors being disposed directly below the bond pad, as recited in Claim 1, 20 and 21. On page 3, lines 10-11 of the originally filed application, it is disclosed that "the active circuit may include a plurality of transistors." Further, Claim 17 of the originally filed application discloses "a plurality of transistors forming a core of circuits." Still yet, on page of 7, lines 16-17 of the originally filed application, it is disclosed that "the bond pads **306** may be disposed above the core **302**, and/or any other part of the active circuit **308**." By virtue of this and other disclosure, applicant's claims clearly meet the written description requirement.

The Examiner has rejected Claims 1, 4-14, 16, 18, 24, 26-27, and 29-30 under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (US Patent Number: 6,707,156) in view of Tanaka (US Patent Number: 6,100,589).

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

With respect to the first element of the *prima facie* case of obviousness, the Examiner states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit of Suzuki et al. having the metal layer defined a frame, such as taught by Tanaka in order to further improve the mechanical strength and to further enhance the effects for suppressing crack formation in the insulation interlayer so that it

inherently prevents the damage to the active circuit and/or the at least one transistor during the bonding process. Applicant respectfully disagrees with this proposition, especially in view of the vast evidence to the contrary.

Specifically, it is noted that Tanaka merely addresses the problem of arranging bonding pads with high density, since a first electrode layer must have a large area in order to secure the bonding area, due to disconnection from bumps of aluminum wiring, etc. Note col. 1, lines 15-45 from Tanaka. Therefore, it is clear that Tanaka simply does not address the problem of bonding-related damage to the active circuit.

Still yet, it is noted that Suzuki does not even mention bonding, let alone the problem of bonding-related damage to the active circuit. Specifically, Suzuki merely teaches a technique for dealing with an increase of stress associated with increasing a height of a multilevel wiring layer structure. For example, Suzuki discloses that "if an interlayer insulating layer of SiOC is disposed between an organic insulating layer and a silicon oxide layer, the generation of stress and the like to be caused by a difference of a physical constant between the upper and lower level layers can be suppressed" (col. 6. lines 11-15). Thus, Suzuki simply does not even address the problem of bonding-related damage to the active circuit.

To this end, neither prior art references even teaches the problem solved by applicant. See *Eibel Process Co. v Minnesota & Ontario Paper Co.*, 261 US 45 (1923). Therefore, for at least the reasons set forth hereinabove, the first element of the *prima facie* case of obviousness has simply not been met.

More importantly, with respect to the third element of the *prima facie* case of obviousness, the Examiner relies on Figure 1 from Suzuki to make a prior art showing of applicant's claimed structure "wherein the [metal layer]... ensures that bonds are capable of being placed over the active circuit" (see this or similar, but not necessarily identical language in each of the independent claims).

Applicant respectfully disagrees with this assertion. First, as mentioned above, Suzuki does not even mention bonding, let alone the problem of bonding-related damage to the active

circuit. Specifically, it is noted that Suzuki merely teaches a technique for dealing with an increase of stress associated with increasing a height of a multilevel wiring layer structure. For example, Suzuki discloses that "if an interlayer insulating layer of SiOC is disposed between an organic insulating layer and a silicon oxide layer, the generation of stress and the like to be caused by a difference of a physical constant between the upper and lower level layers can be suppressed" (col. 6. lines 11-15).

Such disclosure simply does not "ensure that bonds are capable of being placed over the active circuit," let alone "without damage thereto during a bonding process" (emphasis added), as claimed. It appears that the Examiner has admitted to not identifying the above emphasized claim language in the prior art. It also noted that the Examiner appears to rely on an inherency argument by arguing that the resultant combination *inherently* prevents the damage to the active circuit and/or the at least one transistor during the bonding process.

In response, applicant asserts that the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)

Applicant respectfully asserts that the claimed "frame [which] ensures that bonds are capable of being placed over the active circuit without damage thereto during a bonding process" would be *unobvious* in view of the proposed prior art combination, since only applicant teaches and claims the novel use of such framed metal layer structure for the specific purpose of ensuring that bonds are capable of being placed over the active circuit without damage thereto during a bonding process, as claimed.

In summary, none of the references relied upon by the Examiner even suggest a frame, as claimed by applicant, to ensure that bonds are capable of being placed over the active circuit without damage thereto during a bonding process. For these reasons, applicant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the prior art references, when combined, fail to teach or suggest all of the claim limitations, as noted above. It is also asserted that independent Claim 17 is deemed allowable for reasons similar to those set forth hereinabove.

A notice of allowance or a specific prior art showing of all of applicant's claim limitations, in combination with the remaining claim elements, is respectfully requested.